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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,324	01/05/2004	Raminda Udaya Madurawe		1991

33380 7590 07/03/2006

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,324	MADURAWE, RAMINDA UDAYA	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claims 1, 5, 7, 8, 14, and 17 are objected to because of the following informalities:

Claim 1, line 5, "comprises" should be deleted.

Claim 5, line 1, "providing" and "second selectable" should be deleted.

Claim 7, line 1, "The circuit" should be changed to "The IC".

Claim 8, line 1, "comprising" should be changed to "comprising:" and the clause beginning "two selectable" should be placed on the next line in order to clearly distinguish between preamble and body of the claim.

Claim 14, line 2, "of" should be changed to "for" in order to satisfy the 35 USC 112, 6th paragraph requirement for "programmable means".

Claim 17, lines 5, "the pass-gate" should be changed to "the pass-gate logic element".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Duong et al. (US 5,600,264, hereinafter, Duong).

Regarding claim 1, Duong discloses, in Figs. 2-5, an integrated circuit (IC) (col. 1, lines 12+) comprising:

a first selectable fabrication option (SRAM; col. 4, lines 48+) comprised of a user configurable memory circuit: and

a second selectable fabrication option (e.g. antifuse; col. 4, lines 48+) comprised of a hard-wired circuit in lieu of said user configurable memory circuit,

wherein, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options (it is inherent since (e.g.) the path from 120 to any of line 12, 18, 16, or 14 will not be changed, only the memory cells such as 210b will be changed; therefore neither functionality nor performance will be changed).

Regarding claim 2, Duong discloses, in Figs. 2-5, that wherein said first selectable option comprises a configurable Random Access Memory (RAM) module (SRAM; col. 4, lines 48+).

Regarding claim 3, Duong discloses, in Figs. 2-5, that wherein said second selectable option comprises a Read Only Memory (ROM) module (EPROM, EEPROM; col. 4, lines 48+).

Regarding claim 4, Duong discloses, in Figs. 2-5, an input, said input received at an input-pad (inherent input pad in IC; see col. 1, lines 12+); and an output, said output generated at an output-pad (inherent input pad in IC; see col. 1, lines 12+); and an input to output signal propagation delay, said delay substantially identical (path with RAM and path with ROM will be identical when they both have buffered mode; see col. 4, lines 10+, col. 2, lines 6+) between said first and said second selectable fabrication options (col. 4, lines 48+).

Regarding claim 5, Duong discloses, in Figs. 2-5, that wherein said hard-wire circuit comprises at least one custom mask (such as antifuse pull-up and pull-down; col. 4, lines 48+), said at least one mask facilitating:

a power-bus (pull-up to power supply to turn on the NMOS device; see col. 1, lines 50+,

col. 5, lines 20+) connection to replace a logic one in said configurable memory circuit; and a ground-bus (pull-down to ground to turn off the NMOS device; see col. 1, lines 50+, col. 5, lines 20+) connection to replace a logic zero in said configurable memory circuit.

Regarding claim 6, Duong discloses, in Figs. 2-5, wherein said RAM element is selected from one of volatile and non-volatile memory elements (col. 4, lines 48+).

Regarding claim 7, Duong discloses, in Figs. 2-5, wherein said RAM element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements (col. 4, lines 48+).

Regarding claim 8, Duong discloses, in Figs. 2-5, a programmable logic device (PLD) (col. 1, lines 12+) comprising:

two selectable memory construction options (col. 4, lines 48+) to control logic circuits (210a, 220a, 230a, 240a), wherein: a first selectable option comprises a random access memory (RAM) construction (155; col. 4, lines 48+); and a second selectable option comprises a hard-wire read only memory (ROM) construction (155: col. 4, lines 48+), wherein, the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options (since pass transistors 210a, 220a, 230a, 240a will not be changed, only memory can be changed; col. 4, lines 48+).

Regarding claim 9, Duong discloses, in Figs. 2-5, wherein said first selectable option comprises a configuration circuit (col. 4, lines 52+) to configure said RAM.

Regarding claim 10, Duong discloses, in Figs. 2-5, wherein said second selectable option comprises mapping one of said first selectable option RAM bit patterns to a hard-wire ROM

pattern (col. 4, lines 48+).

Regarding claim 11, Duong discloses, in Figs. 2-5, an input, said input received at an input-pad (inherent input pad in IC; see col. 1, lines 12+); and an output, said output generated at an output-pad (inherent input pad in IC; see col. 1, lines 12+); and an input to output signal propagation delay, said delay substantially identical (path with RAM and path with ROM will be identical when they both have buffered mode; see col. 4, lines 10+, col. 2, lines 6+) between said RAM and said ROM logic control options (col. 4, lines 48+).

Regarding claim 12, Duong discloses, in Figs. 2-5, wherein said RAM element is selected from one of volatile and non-volatile memory elements (col. 4, lines 48+).

Regarding claim 13, Duong discloses, in Figs. 2-5, wherein said RAM element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements (col. 4, lines 48+).

Regarding claim 14, Duong discloses, in Figs. 2-5, a pass-gate logic element (col. 3, lines 40+), said logic element providing a programmable means for electrically connecting or disconnecting two nodes (see fig. 5).

Regarding claim 15, Duong discloses, in Figs. 2-5, wherein said programmable means in said first selectable option comprises configuring a RAM bit (col. 4, lines 48+), said RAM bit generating: a logic one output to connect said two nodes (with NMOS device, "1" to turn on; see col. 1, lines 50+, col. 5, lines 20+); and a logic zero output to disconnect said two nodes (with NMOS device, "0" to turn off).

Regarding claim 16, Duong discloses, in Figs. 2-5, wherein said programmable means in

said second selectable option comprises hard-wiring a ROM bit (such as antifuse pull-up and pull-down; col. 4, lines 48+), said ROM bit providing: a hard-wire to power-bus (pull-up to power supply to turn on the NMOS device; see col. 1, lines 50+, col. 5, lines 20+) to connect said two nodes; and a hard-wire to ground-bus (pull-down to ground to turn off the NMOS device; see col. 1, lines 50+, col. 5, lines 20+) to disconnect said two nodes.

Claims 17-20 are essentially the same as claims 1-16 as discussed above and are rejected similarly.

Response to Arguments

Applicant's arguments filed 4/17/2006 have been fully considered but they are not persuasive.

Applicant argues that Duong disclosure does not pertain to logic circuits or interconnect structure that is invariant to the memory choice, nor timing exactness between multiple programmable memory choices. However, Duong discloses that the memory cells of switch box 155 can be SRAM, EPROM, EEPROM, flash memory, antifuse pull-up or pull-down, or composed of a number of other well known programmable memory cells. Memory cells 210b, 220b, 230b, 240b... are programmed during the initialization operation to configure switch box 155 (col. 4, lines 48+). This can be interpreted that the IC of Duong is comprised of a first selectable fabrication **option** comprised of a user configurable memory circuit such as SRAM coupled with the pass gates 210a, 220a, 230a, and 240a. Also, it can be interpreted that this same IC of Duong is comprised of a second selectable fabrication **option** with a hard-wired circuit such as ROM or antifuse in lieu of said memory circuit. Since the word, "option" means

"choice" according to MSN dictionary, the IC does not have to have "a single PLD that comprises two selectable memory constructions" as applicant argues. Also, Duong discloses that the memory cells of switch box 155 can be any of the well known programmable memory cells and silence about the pass transistors 210a, 220a, 230a, and 240a being switchable. This means that no components on the path from one point to the other (e.g. from output of 120 to any line of 12, 18, 16, or 14 having pass gates 210a, 220a, 230a, and 240a in between) will be changed. Only the programmable memory cells can be changed. Consequently, there will be no time differences or delay on the same paths for the two different options. Therefore, the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options and the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options as set forth in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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dc

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PRIMARY EXAMINER